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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

pplicant:

Kiran Ganesh et al.

Examiner:

Phallaka Kik

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Title:

2-DIMENSIONAL PLACEMENT WITH RELIABILITY CONSTRAINTS FOR

VLSI DESIGN

Assignee: Intel Corporation

AMENDMENT UNDER 37 C.F.R. §1.116

Mail Stop RCE Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

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Please amend the above-identified patent application as follows.

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